IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of:		
	Pankaj Kedia	
Serial No.:	09/753,326	Art Unit: 2116
Filed:	December 29, 2000	
		Examiner: Chen, Tse W.
For:	Low Power Subsystem For Portable Computers	

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicants (hereafter "Appellants") hereby submit this Brief in support of its appeal from a final decision by the Examiner, mailed November 6, 2006 in the above-captioned case. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

An oral hearing is not desired.

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I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052-8119.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences that are related to, will directly affect, will be directly affected by, or have a bearing on the Board's decision in the present appeal.

III. STATUS OF THE CLAIMS

Claims 29-56 are currently pending in this application. Claims 1-28 have been canceled. No claims have been allowed. All pending claims were rejected as obvious in the final Office action mailed November 6, 2006 and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action mailed on November 6, 2006, rejecting claims 29-56, Appellants file herewith a Notice of Appeal and this Brief.

A copy of all claims on appeal is attached hereto as Appendix A.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Claims

Claim 29 is presented as a method with the following elements:

transitioning a central processing unit (CPU) (102 Page 4, line 9) of a computer system (100, Page 4, line 8) into a low power mode (See page 3, lines 3-6, lines 12-15,), the computer system having a memory (105 Page 4, line 18),

activating a low power subsystem (110 Page 5, line 11) when the CPU enters the low power mode, the low-power subsystem including a low power processor (111 Page 5, line 11), an external interface (115 Page 5, line 18) and a low power memory (113 Page 5, line 13);

independent of the CPU (See page 3, lines 7-10, , using the low power processor of the low power subsystem to access data contained within the computer system memory (See page 3, line 21-page 4, line 1, page 5, lines 17-22, page 6, lines 1-6, lines 15-16); and

providing the accessed data through the external interface of the low-power subsystem.

Claim 38 is presented as an apparatus with primarily the same features as Claim 29.

a computer system (100, Page 4, line 8) having a central processing unit (102 Page 4, line 9), a system memory (103 Page 4, lines 10-11), a mass storage device (105 Page 4, line 18), and a user interface, the computer system having a low-power mode (See page 3, lines 3-6, lines 12-15,); and

a low-power subsystem (110 Page 5, line 11) in operation when the computer system enters the low-power mode, the low power subsystem having a low power processor (111 Page 5, line 11), a low power subsystem memory (113 Page 5, line 13) and an external interface (115 Page 5, line 18) independent of the computer system, the low power processor providing access (See page 3, line 21-page 4, line 1, page 5, lines

17-22, page 6, lines 1-6, lines 15-16) to the computer system when the computer system is in the low power mode and the external interface providing data accessed from the computer system externally.

Claim 51 is directed only to the low power subsystem portion of Claim 29.

a miniature display screen (115, Page 5, lines 15-16);

a user input unit (this may be implemented through the Bluetooth interface 116 with an antenna 130 (See page 4, lines 2-4). A microphone may also be used (See page 7, lines 5-8));

a low-power subsystem memory (113 Page 5, line 13); and

a low-power processor (111 Page 5, line 11) coupled to the miniature display screen, to the user input unit, and to the memory, the low-power processor providing access (See page 3, line 21-page 4, line 1, page 5, lines 17-22, page 6, lines 1-6, lines 15-16) for the miniature display screen and the user input unit to a connected computer system (100, Page 4, line 8) when the connected computer system is in a low-power mode.

Background

The invention of Claim 1 may be easily understood in the context of the Background section of the present invention and in view of paragraph 5 which reads as follows.

"A low-power subsystem for a portable computer, which operates while the computer is in a low-powered mode in which the CPU performs in a less active state, is disclosed. Normally, when the notebook computer is in low power mode (also called powered down mode) during which the CPU is in a less active state and the notebook display screen may be in the closed position, the data stored within the computer typically cannot be accessed. One embodiment described herein allows access to the data while the computer is low power mode by use of a low-power subsystem (LPS) in the computer with access to the same memory storage as the CPU. The subsystem acts

independently of the CPU, which would not be able to perform the necessary functions during low power mode. The subsystem allows the notebook to perform several functions while in the low power mode, such as, for example, act like a travel assistant for the user, provide entertainment, and make electronic purchases."

VI. GROUNDS OF REJECTION

The drawings are objected to under 37 CFR 1.83(a) as failing to show every feature of the invention specified in the claims.

(A) Claims 29, 31 and 32 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Umina, U.S. Patent 5,287,485 ("Umina"), in view of Barber, U.S. Patent No. 6,240,521 ("Barber").

(B) Claim 30 stands rejected under 35 U.S.C. §103 (a) as being unpatentable over Umina, in view of Barber, and in further view of Kableshkov, U.S. Patent No. 6,108,663 ("Kableshkov").

(C) Claims 33-34, 36 and 37 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Umina, in view of Barber, and in further view of Ditzik, U.S. Patent No. 5,983,073 ("Ditzik").

(D) Claim 35 stands rejected under 35 U.S.C. §103 (a) as being unpatentable over Ditzik, Umina, Barber, and in further view of Chen, U.S. Patent No. 5,590,197 ("Chen").

(E) Claims 38, 43, 45-51 and 54-56 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Ditzik, in view of Kim, U.S. Patent No. 6,044,473 ("Kim").

(F) Claims 39-42, 44, and 52-53 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Ditzik and Kim, and in further view of Kableshkov.

The drawings were also objected to, as noted below.

Grounds C and D are not argued below.

VII. ARGUMENT

A. The drawings objection is six Office actions late and should be dismissed as exemplary of piecemeal examination or, in the alternative, administered on remand through a non-final action.

The Examiner has objected to the drawings as failing to show "activating a low power subsystem when the CPU enters the low power mode" and "independent of the CPU, using the low power processor of the low power subsystem to access data contained within the computer system memory."

Claim 1 of the originally filed application recites, "transitioning a processing unit of a computer system into the low power mode and after the processing unit has transitioned into the low power mode, accessing data contained within a memory device of the computing system, via a low-power subsystem."

This original Claim 1 clearly refers to (a) the low power subsystem being active when the CPU enters the low power mode, and (b) using the low power subsystem to access data contained within the computer system memory.

"Independent of the CPU" was added to the claims in response to the third Office action in a response filed June 1, 2005. "Activating... when the CPU enters the low power mode" was added to the claims in the second RCE filed September 20, 2005, in response to the sixth Office action

The outstanding objection is the ninth Office action (not counting Advisory Actions) in the present application and the first one to object to the drawings. Each Office action has been issued by the same Examiner. 37 C.F.R. §104(a) states that, on taking up an application for examination, the examiner shall make a thorough study thereof. The examination shall b e complete with respect both to compliance of the application with the applicable statutes and rules and to the patentability of the invention as claimed, as well as with respect to matters of form. 37 C.F.R. §104(b) states that the

Examiner's action will be complete as to all matters (subject to some inapplicable exceptions). For this reason, the M.P.E.P warns examiners against piecemeal examination.

As to drawings, M.P.E.P. §608.02 provides for two situations: those that fall under 35 U.S.C. §113 first sentence; and those that fall under 35 U.S.C. §113, second sentence. The examiner has clearly treated this as a second sentence situation in which case, the standard becomes that "the nature of such subject matter admits of illustration by a drawing." This is appropriately a subjective standard that falls within the discretion of the Office.

New drawings have been required for the first time on a ninth substantive Office action and, at the least, on the third Office action after the claims acquired their present form. Such a late requirement does not reflect the high standards of quality, competence, and compliance typical of this Office. While, by its very nature, the Board does not see a representative example of excellent examiners performing their job well, it is Appellant's experience that such a late requirement is an anomaly. For this reason, Appellants respectfully request that the subjective requirement be withdrawn in order to uphold the high standards with which most examiners comport and which the proper function of the Office demand.

If the Board feels that the public interest would be served by adding the required drawing to the present application, Appellants are happy to do so on remand and ask only that the first Office action on remand not be final to allow Applicants sufficient time to reach agreement with the Examiner on the nature of the new drawing.

B. Claim 29 is not obvious where neither reference teaches or suggests "using the low power processor of the low power subsystem to access data contained within the computer system memory."

Claims 29, 31 and 32 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Umina, U.S. Patent 5,287,485 ("Umina"), in view of Barber, U.S. Patent No. 6,240,521 ("Barber"). Barber was relied on in the first Office action of November 20, 2003 and has remained the primary focus of the prosecution of the present application throughout.

The Examiner would like to present this as a new rejection, however, it is not. The Examiner has cited Umina as showing (a) a computer system having a CPU 202 and a memory 204, and (b) a subsystem including a processor 206 and a memory 208. (The Examiner indicates that the subsystem is low power, but then writes that "Umina did not disclose low power operations.") Going back to November 20, 2003, this same Examiner on page 3 states that Barber shows the same thing. The combination of Barber with a reference that is relied on to show what was already stated to be in Dwyer is not a new rejection.

Umina has two SRAMs 204, 208 and two processors 202, 206. Both processors can access either SRAM, but only one at a time and only if the connections are reversed. (Col. 5, lines 41-62) Transfer logic 270 lies in between the two SRAMs described with respect to Figure 7, but not between the processors and the SRAMs. Umina, as suggested by the Examiner, has no low power operation. It is directed instead at high speed dual processor operation. The difference between Umina and Barber is that Umina shows two high power processors each with their own memory, while Barber, on the other hand has a low power processor that shares a single memory with a high speed processor.

Barber shows a conventional computer system with two processors 42, 44 coupled to a single I/O bus 46. In Barber, two processors share "a common instruction set and address space." "Since the two processors share a common address space, the contents of memory is available equally to both processors. It is only the machine state which must be passed back and forth between the active processor via the shared memory and the sleep mode transitions." (Col. 3, lines 43 et seq.)

In other words, the processors share everything. While this reduces the component price for the system, it increases the power consumption. In Barber, it provides for seamless transitions between the two processors.

In Claim 29, there are two processors but the low-power subsystem has its own memory. It also has its own external interface ("the low-power subsystem including a low power processor, an external interface and a low power memory"). Neither reference shows a whole subsystem. The components of the low power subsystem of the present invention may be optimized for low power operation, while the memory and external interface of the "computer system" may be optimized for speed. This costs more than reusing the same components but it provides a longer battery life. The low-power subsystem only has to access the "computer system" when data located there is desired.

Claim 29 further recites "using the low power processor of the low power subsystem to access data contained within the computer system memory." This draws a clear distinction between the computer system memory and the low-power subsystem memory. In Barber, there is only one memory, while in Umina, there is no low power subsystem.

Claim 29 further recites, "providing the accessed data through the external interface of the low-power subsystem." This operation is not possible with either reference as there is no separate external interface for the second processor.

In sum, neither reference shows a low power subsystem, only a second processor.

The Examiner could have argued that it would be obvious to apply the high power/low power system of Barber to the dual memory/dual processor system of Umina. Umina is directed to sharing data in the two memories between the two processors as quickly as possible. (See e.g. Col. 1, lines 50-65) Umina solves the problem using the transfer logic 270 that allows for direct transfer of data from one memory to another. Claim 29 recites, "using the low-power processor of the low-power subsystem to access data contained within the computer memory system." To the extent that this can be read

on Umina. Umina considers this option and rejects it at Col. 1, lines 50-65 in favor of its transfer logic solution. To make such a modification of Umina then goes against the teachings of Umina and reduces its performance for the reasons that Umina provides.

The Examiner could have argued that it would be obvious to apply the dual memory/dual processor system of Umina to the high power/low power system of Barber. Barber, however, relies heavily on a saved machine state that is used to transition between the two processors (Abstract). Saving the current machine state in the shared address space allows for seamless transitions between the high and low power processors. Adding the second memory space would defeat the shared address space and defeat the entire purpose of Barber. The processors would no longer be able to make the seamless transitions.

If there is some way to add the memory and keep the shared address space, it is not described in either reference and it would require some significant design or engineering to accomplish. Umina does not discuss how to switch between processors but only contemplates using both processors at the same time and so provides no help in how to add a second memory without destroying the shared address space.

Neither singly, nor in combination, do the references teach or suggest the claimed invention. Accordingly, Appellants respectfully request that the Board reverse the Examiner's rejection of Claims 29, 31, and 32.

C. Claim 30 is not obvious where none of the references teach or suggest "a shared database with at least a partial copy of [the] data."

Claim 30 stands rejected under 35 U.S.C. §103 (a) as being unpatentable over Umina, in view of Barber, and in further view of Kableshkov, U.S. Patent No. 6,108,663 ("Kableshkov"). The application of Kableshkov to this claim is not new. Claim 30 refers to "accessing data comprises accessing data through a shared database of the low-power

subsystem, the method further comprising storing at least a partial copy of data accessed from the computer system memory in the shared database."

Kableshkov was cited as showing a shared database. However, Kableshkov does not show a shared database as recited in Claim 30. On the contrary, there is a single data source 34 that is accessed either by the co-processor 40 or both the co-processor and the host processor 30 through a common I/O bus. This does not correspond to a shared database through which access to a computer system may be provided. It does not suggest a computer system memory, a low-power subsystem memory, and a shared database in combination.. Further there is nothing in any of these three references to suggest modifications to accomplish such a thing. There is also nothing in any of the references to suggest applying such a database to allow a high speed processor to remain in a low power state.

Appellants accordingly request that the rejection of Claim 30 also be reversed.

D. Claims 38 and 51 are not obvious when neither reference suggests "activating a low-power subsystem when the [computer system] CPU enters the low-power mode'"

The Examiner has rejected claims 38, 43, 45-51 and 54-56 under 35 U.S.C. §103 (a) as being unpatentable over Ditzik, U.S. Patent 5,983,073 ("Ditzik"), in view of Kim, U.S. Patent No. 6,044,473 ("Kim"). This rejection was fully addressed in Appellant's previous brief.

Claim 38, for example, recites, " a low-power subsystem in operation when the computer system enters the low-power mode."

Ditzik shows a modular portable device that combines a notebook computer, cellular telephone, and tablet PC into a single housing. The modules are best seen in Figure 2. The tablet/display 2 is held onto a cover assembly 8, 9, 16 by an expandable hinge 10. The cover assembly can be separated into its respective three pieces. The first

piece 9 is the battery, the middle piece 16 is the keyboard and the third piece 8 carries a "wireless handset" 14 that supports typical cellular telephone standards (Column 5, line 57).

The only interaction between the wireless handset and the rest of the system that is suggested anywhere in Ditzik is that the base unit 100 can act as an RF repeater (see e.g. 8:32-58)). The telephone is summarized at 8:19-25. It is simply a cellular telephone. Ditzik never discloses or suggests that any components of the telephone (except perhaps for some radio components and the display) are less than fully-powered and operational all the time.

Kim is cited only for showing that a computer may have a low power mode. In Kim, the notebook computer enters the low power mode when the lid is closed due to a concealed switch (See, e.g. ABSTRACT and Description of the Related Art.)

In the Response to Arguments section of the March 16, 2006 Office action, the Examiner agrees that Kim does not show a low-power subsystem. The Examiner relies upon Ditzik for this teaching. The Examiner appears to assert that Ditzik discloses a telephone 14 as a low-power subsystem.

The Examiner would appear to be arguing that the fully powered telephone 14 is a low-power subsystem that can operate with the base station 100 system memory 40, 42 while the base station 100 and its CPU 38 are in the low-power mode of Kim.

Claim 38 recites, "a low-power subsystem in operation when the computer system enters the low-power mode." This is not taught or suggested in either reference. The only way to achieve such an operation is to switch a modified Ditzik computer 100 in Kim's low power mode and to then turn on the telephone 14 at about the same time. While it may be possible for a user to do this, there is no motivation to do so in either reference. Accordingly, this limitation of Claim 38 is not met by the references alone or in combination.

E. Claim 38 and 51 are not obvious when neither reference suggests "the low power processor providing access to the computer system when the computer system is in the low power mode."

In the Response to Arguments section of the March 16, 2006 Office action, the Examiner agrees that Kim does not show a low-power processor that acts independently of the CPU. The Examiner again relies upon Ditzik for this teaching. The Examiner appears to assert that the telephone in Ditzik interfaces with a user to access data in the notebook computer section without the CPU 38 (microprocessor 38 of Figure 7, not interface slot/connector 38 of Figure 2).

The Examiner would appear to be arguing that the fully powered telephone 14 is a low-power subsystem that can operate with the base station 100 system memory 40, 42 while the base station 100 and its CPU 38 are in the low-power mode of Kim.

Regarding this limitation, the Examiner cites Ditzik at 8:4-58, 9:55-10:10, and 13:1-30. None of these sections suggest that the telephone 14 may be used to access data in the system memory 40, 42, nor that it be able to access such data when the CPU 38 is in a low power mode. (Ditzik has no other memory to access than the items 40, 42, shown in Figure 7.) The only interaction between the wireless handset and the rest of the system that is suggested anywhere in Ditzik is that the base unit 100 can act as an RF repeater (see e.g. 8:32-58)). This would not involve accessing data within the base unit.

Claim 38 recites, "the low power processor providing access to the computer system when the computer system is in the low power mode."

Claim 38 further recites, "providing data accessed from the computer system externally." Since the telephone 14 is not capable of accessing data in the computer 100, it is further incapable of providing such accessed data in any way.

Since Kim does not show a low-power subsystem, it does not add anything to this aspect of the rejection. Accordingly, this limitation of Claim 38 is also not met by the references alone or in combination.

All other claims are believed to be allowable on the grounds presented above. The Examiner does not cite any of the other references for the teachings of the independent claims 38 and 51. Accordingly, Appellants request that this rejection also be reversed.

F. **Claims 39 and 52 are not obvious where none of the references teach or suggest "the low power processor access the computer system through the shared database."**

Claims 39-42, 44, and 52-53 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Ditzik and Kim, and in further view of Kableshkov. Kableshkov has previously been applied to these claims. Claim 39, for example, refers to " a shared database coupled to the computer system and to the low-power subsystem and wherein the low power process[or] accesses the computer system through the shared database."

Kabelshkov was cited again as showing a shared database. As mentioned above, Kabeshkov does not show a shared database as recited in Claim 39. Appellants accordingly request that the rejection of Claims 39 and 52 and the related claims also be reversed.

VIII. CONCLUSION

Appellants respectfully submit that all the appealed claims in this application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

Please charge any shortages and credit any overpayment to out Deposit Account No. 02-2666.

Respectfully submitted,

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Date: February 6, 2007

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APPENDIX OF CLAIMS (37 C.F.R. § 1.192(c)(7))

29. A method comprising:

transitioning a central processing unit (CPU) of a computer system into a low power mode, the computer system having a memory,

activating a low power subsystem when the CPU enters the low power mode, the low-power subsystem including a low power processor, an external interface and a low power memory;

independent of the CPU, using the low power processor of the low power subsystem to access data contained within the computer system memory; and

providing the accessed data through the external interface of the low-power subsystem.

30. The method of Claim 29, wherein accessing data comprises accessing data through a shared database of the low-power subsystem, the method further comprising storing at least a partial copy of data accessed from the computer system memory in the shared database.

31. The method of Claim 29, wherein accessing data contained within the computer system memory comprises accessing data contained within a disk drive unit.

32. The method of claim 31, wherein the data contained in the shared database includes multimedia data.

33. The method of claim 29, further comprising accessing data from a network via the external interface of the low-power subsystem.

34. The method of claim 33, wherein accessing data from the network comprises accessing data from the network using a wireless interface.

35. The method of claim 33, wherein accessing data from the network comprises accessing data from ~~is~~ an electronic store allowing an electronic purchase.

36. The method of claim 29, wherein providing the accessed data through the external interface comprises presenting the data accessed to a user via a display of the external interface of the low-power subsystem.

37. The method of claim 29, wherein providing the accessed data through the external interface comprises presenting the data accessed to a user via an audio medium of the external interface of the low-power subsystem.

38. An apparatus comprising:

a computer system having a central processing unit, a system memory, a mass storage device, and a user interface, the computer system having a low-power mode; and

a low-power subsystem in operation when the computer system enters the low-power mode, the low power subsystem having a low power processor, a low power subsystem memory and an external interface independent of the computer system, the low power processor providing access to the computer system when the computer system is in the low power mode and the external interface providing data accessed from the computer system externally.

39. The apparatus of Claim 38, further comprising a shared database coupled to the computer system and to the low-power subsystem and wherein the low power processes accesses the computer system through the shared database.

40. The apparatus of Claim 39, wherein the computer system memory ~~device~~ comprises a random access memory coupled to the central processing unit, and wherein the computer system mass storage device comprises a disk drive unit coupled to the central processing unit.

41. The apparatus of Claim 40, wherein the shared database is coupled to the disk drive unit, the shared database to store at least a partial copy of data stored on the disk drive unit.

42. The apparatus of claim 39, wherein data contained within the shared database includes multimedia data.

43. The apparatus of claim 38, wherein the low-power subsystem external interface comprises a wireless interface ~~is~~ to connect with a local area network.

44. The apparatus of claim 39, wherein the low power subsystem external interface comprises a video display to display data from the shared database.

45. The apparatus of claim 38, wherein the external interface of the low-power subsystem further comprises a wireless user interface to receive verbal commands from a user.

46. The apparatus of claim 45, wherein the wireless user interface further comprises an audio headset to receive audio data transmitted from the wireless user interface.

47. The apparatus of claim 38, wherein the low-power subsystem external interface further comprises an interface to transmit data to a cellular phone.

48. The apparatus of claim 38, wherein the computer system comprises a main screen and the low-power subsystem comprises a miniature display screen and wherein the low-power subsystem including the miniature display screen is activated when the main screen is closed.

49. The apparatus of claim 38, wherein the computer system comprises stored multimedia data, wherein the low-power subsystem accesses the stored multimedia data

and wherein the low-power subsystem presents the multimedia data to a user through the external interface.

50. The apparatus of claim 49, wherein the low-power subsystem presents the multimedia data to the user over a miniature display screen of the external interface.

51. A low-power subsystem comprising:

a miniature display screen;

a user input unit;

a low-power subsystem memory; and

a low-power processor coupled to the miniature display screen, to the user input unit, and to the memory, the low-power processor providing access for the miniature display screen and the user input unit to a connected computer system when the connected computer system is in a low-power mode.

52. The low-power subsystem of claim 51 wherein the processor provides access to the computer system through a shared database, the shared database being a part of the low-power subsystem.

53. The low-power subsystem of claim 52, wherein the shared database is coupled to the computer system to store at least a partial copy of data stored in the computer system.

54. The low-power subsystem of claim 51, further comprising a wireless interface to connect to an external network.

55. The low-power subsystem of claim 51, further comprising a wireless interface to connect the user input unit and the processor.

56. The low-power subsystem of claim 51 wherein the user input unit comprises a wireless user interface to receive verbal commands from a user.

XI. EVIDENCE APPENDIX

None.

XII. RELATED PROCEEDINGS APPENDIX

None.